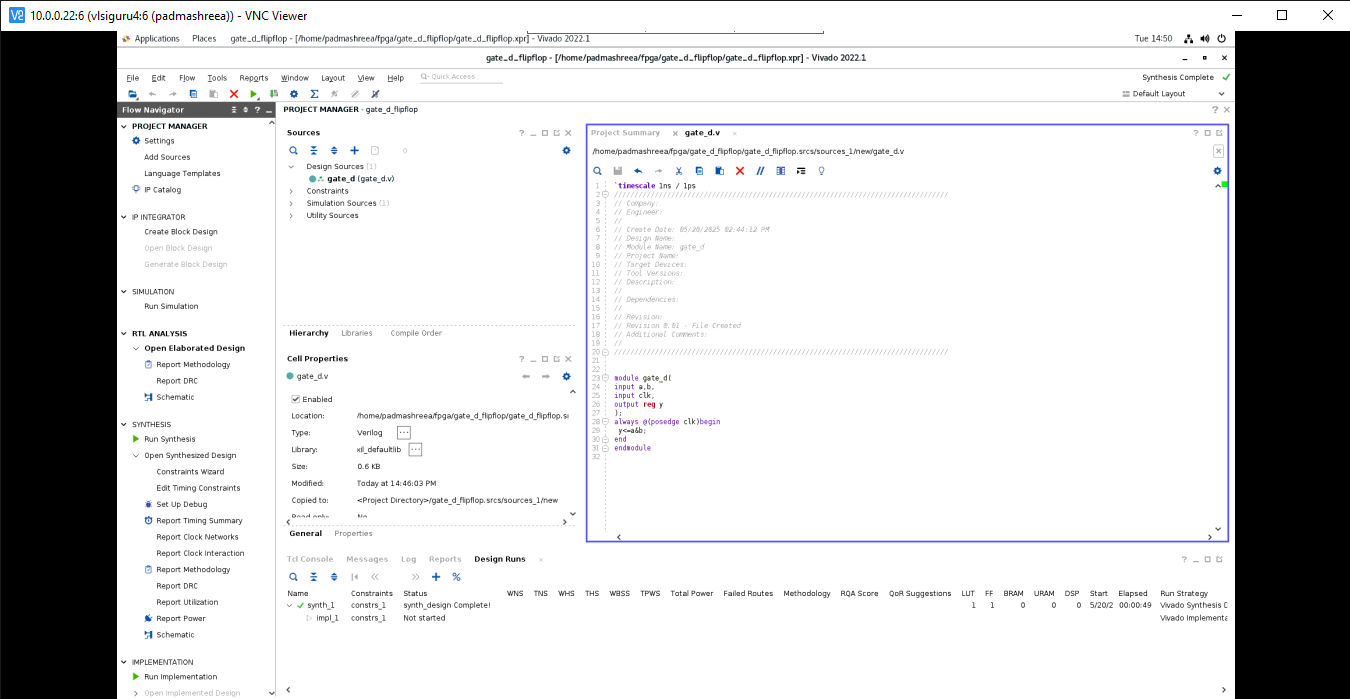
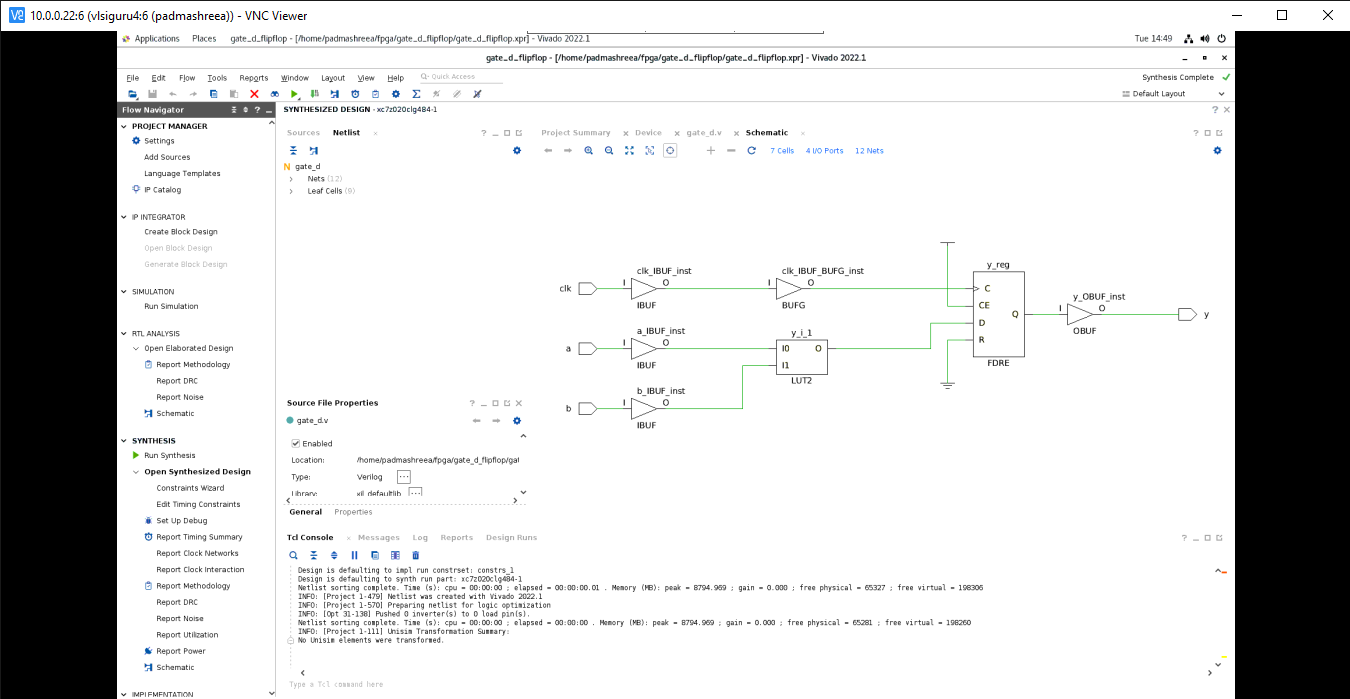
**Session 2**

**Implement AND gate with d flipflop**

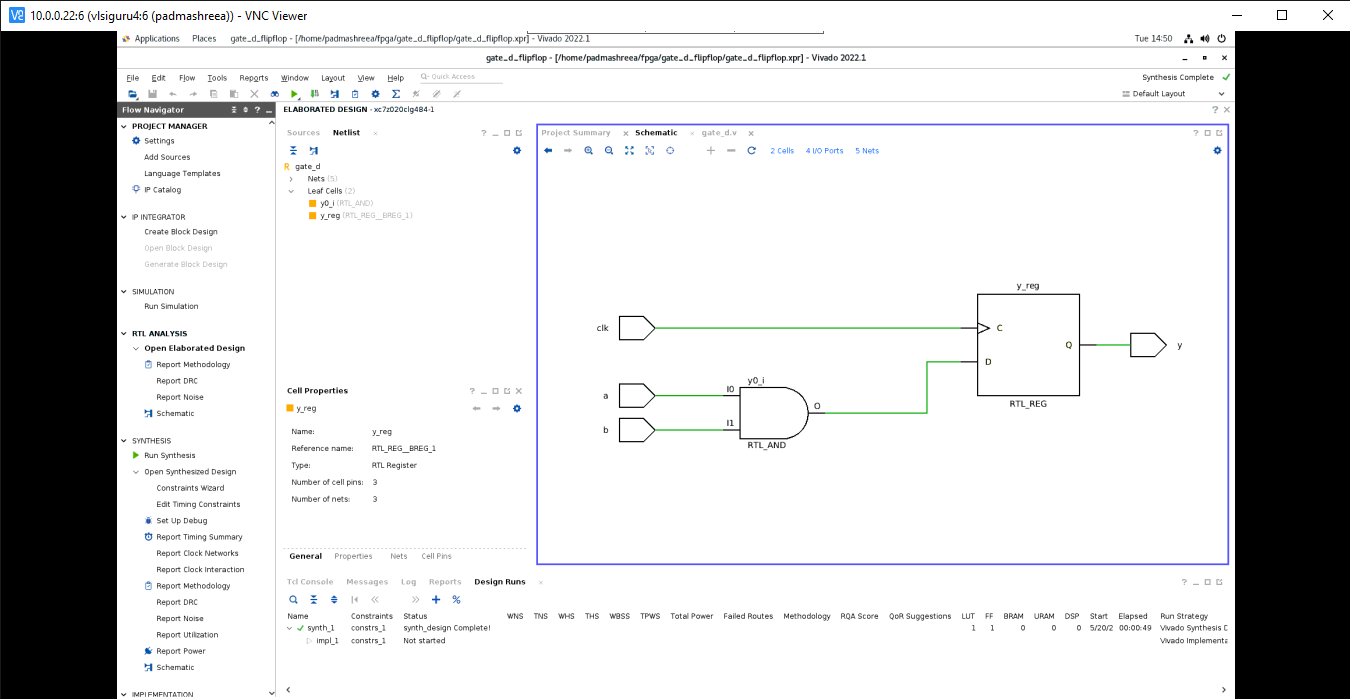
**RTL/Verilog code:**

****

**Schematic diagram**

****

**Elaborated circuit:**

****

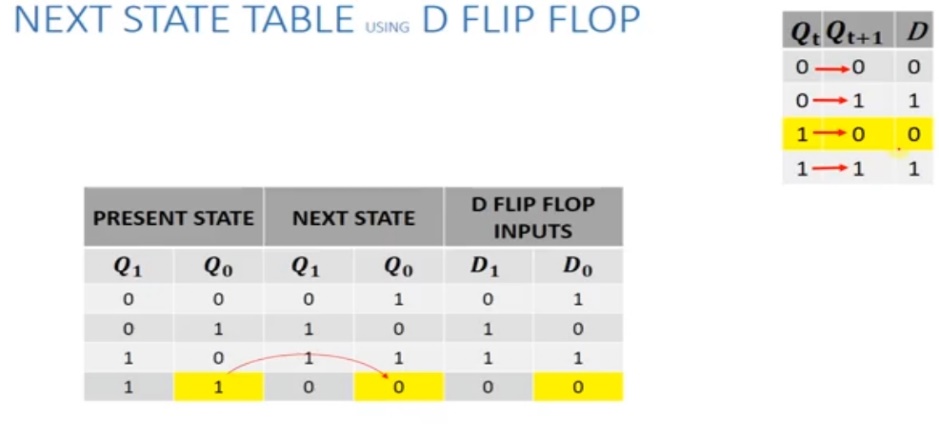
**Implement 2-bit counter using LUT and flipflop**

For counter using flip flop, first we have to draw table for present state and next state for up-counter then d flip-flop excitation table. By using excitation table of d flipflop we have to write d flip-flop outputs.

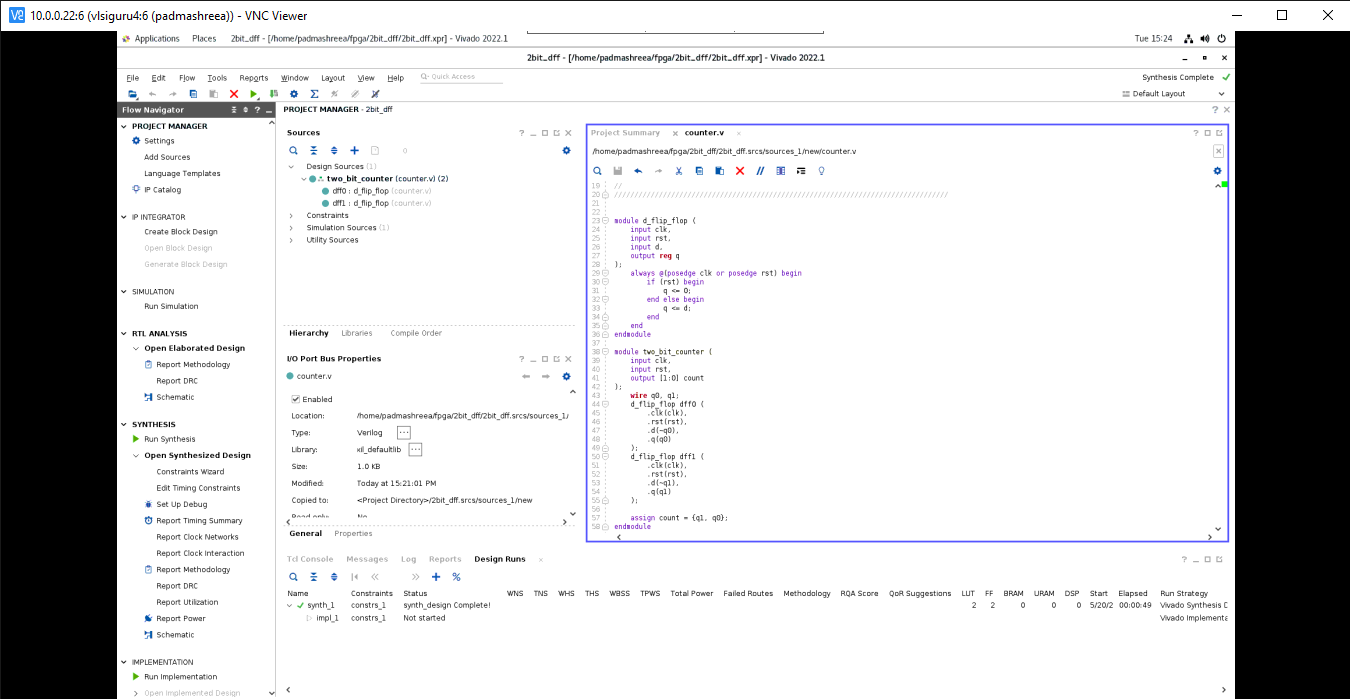
Then using k-map we have to deduce equation for D1 and D2, As follows

D1 = Q1 xor Q0

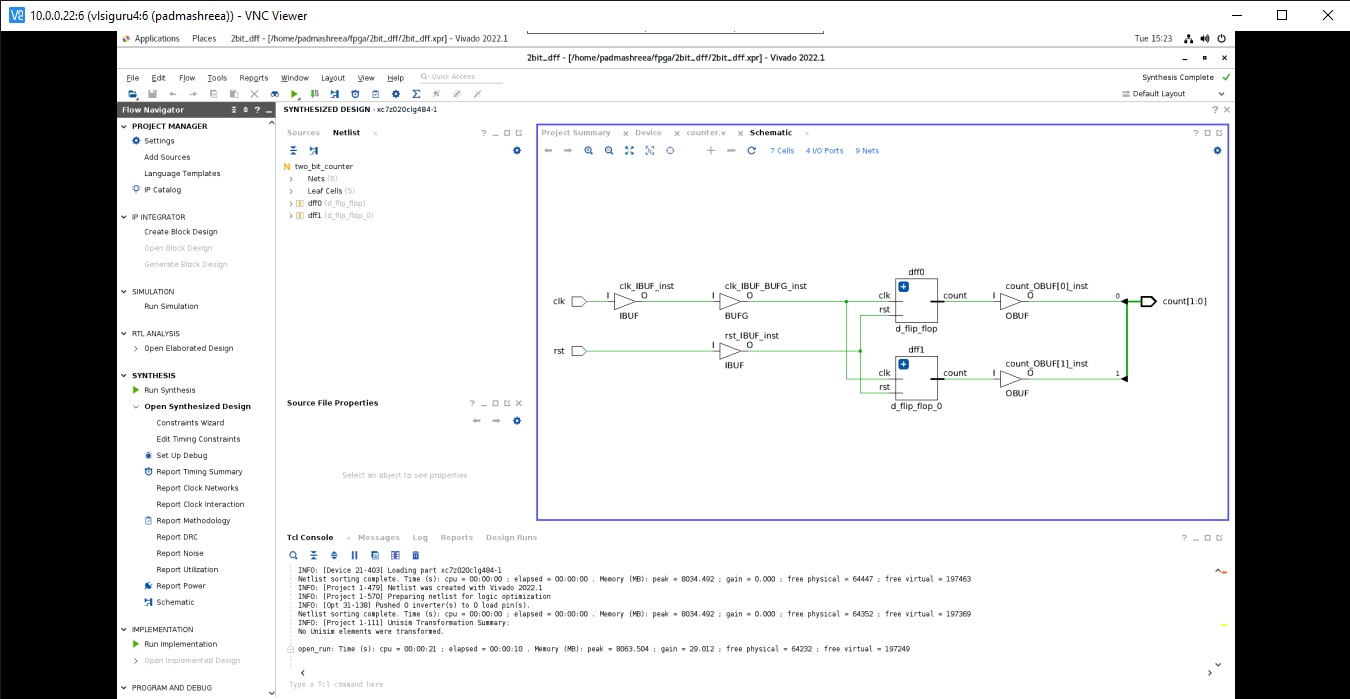
D0 = Q0’



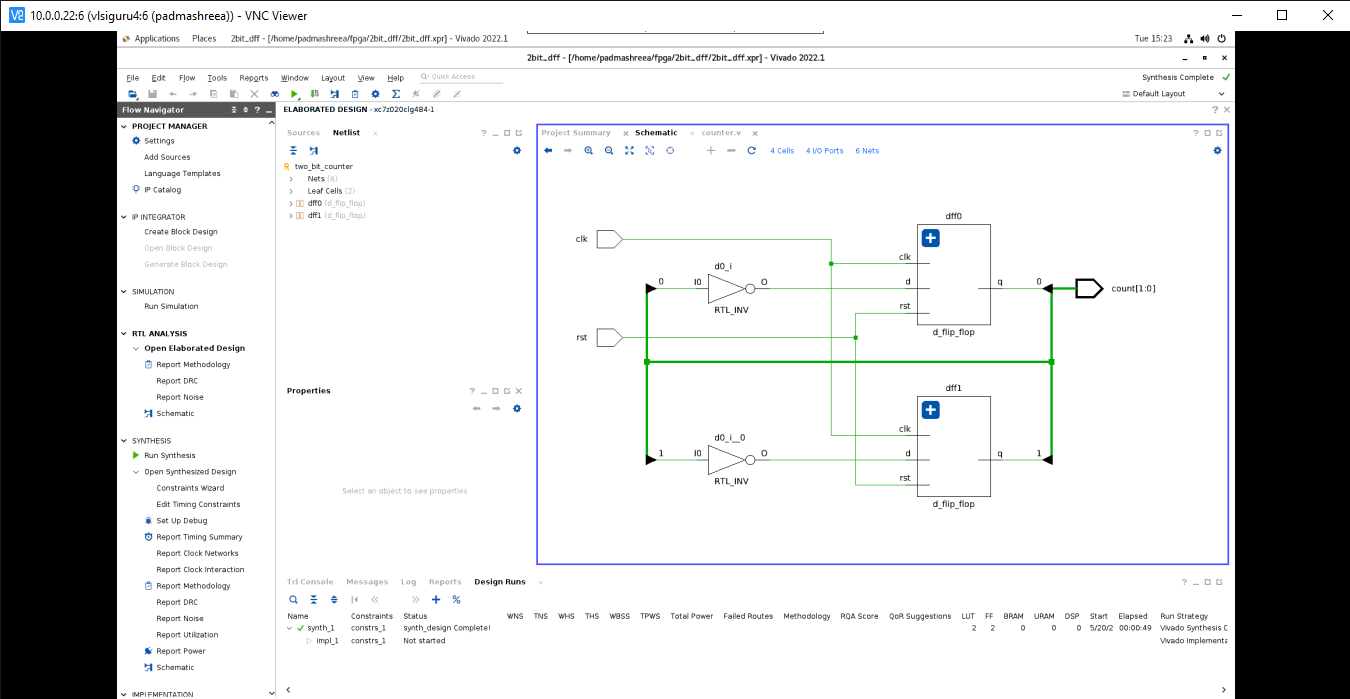
**RTL/Verilog code:**

****

**Schematic diagram:**

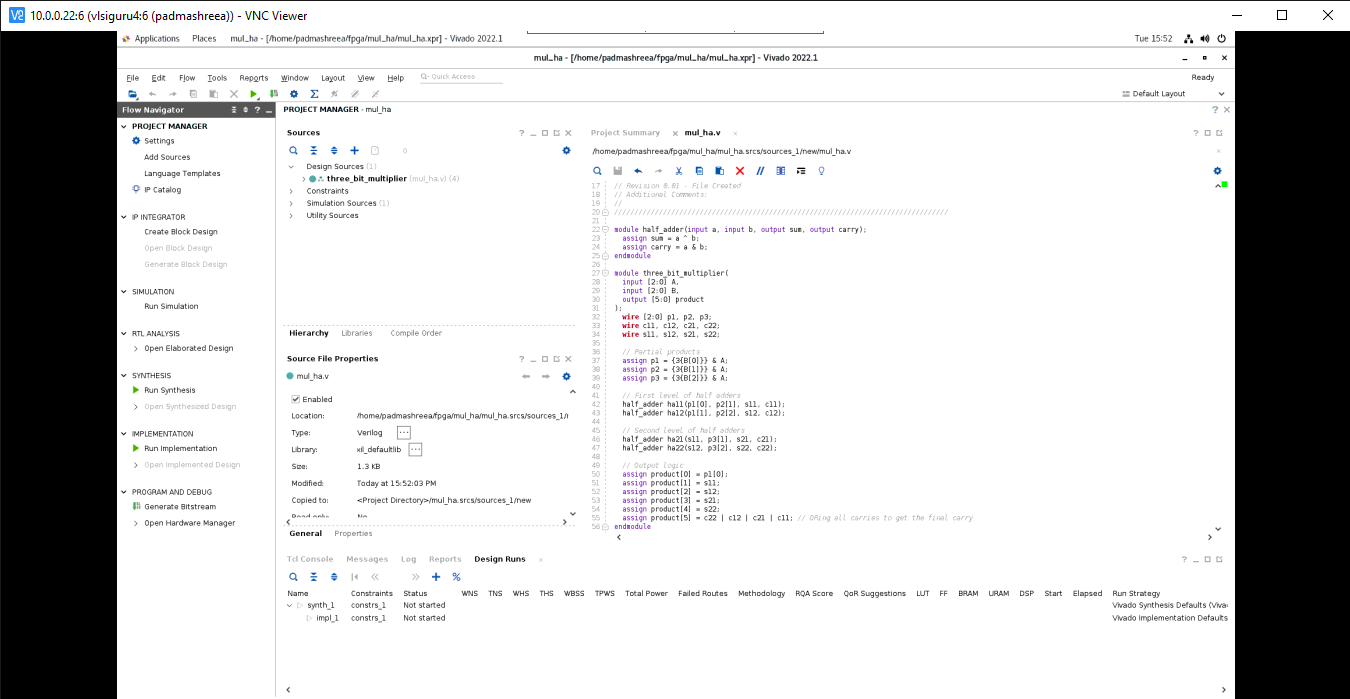
****

**Elaborated circuit:**

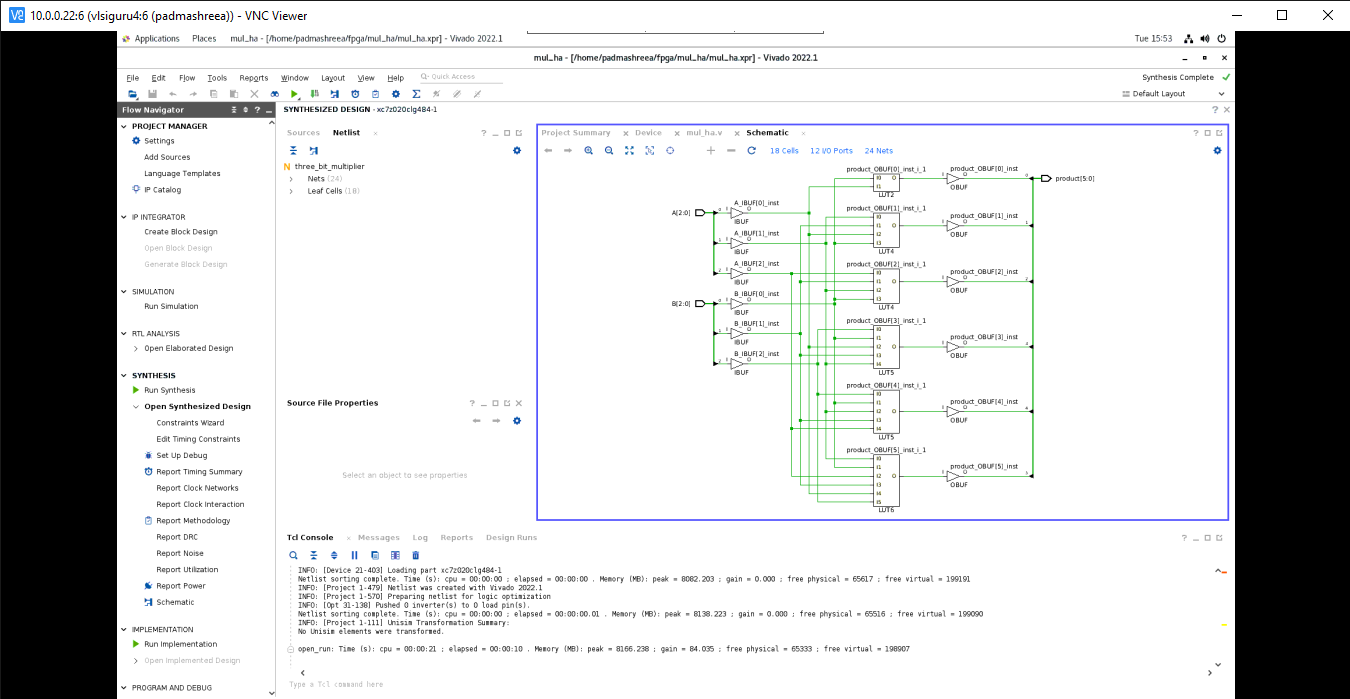
****

**Implement 3-bit multiplier using half adder**

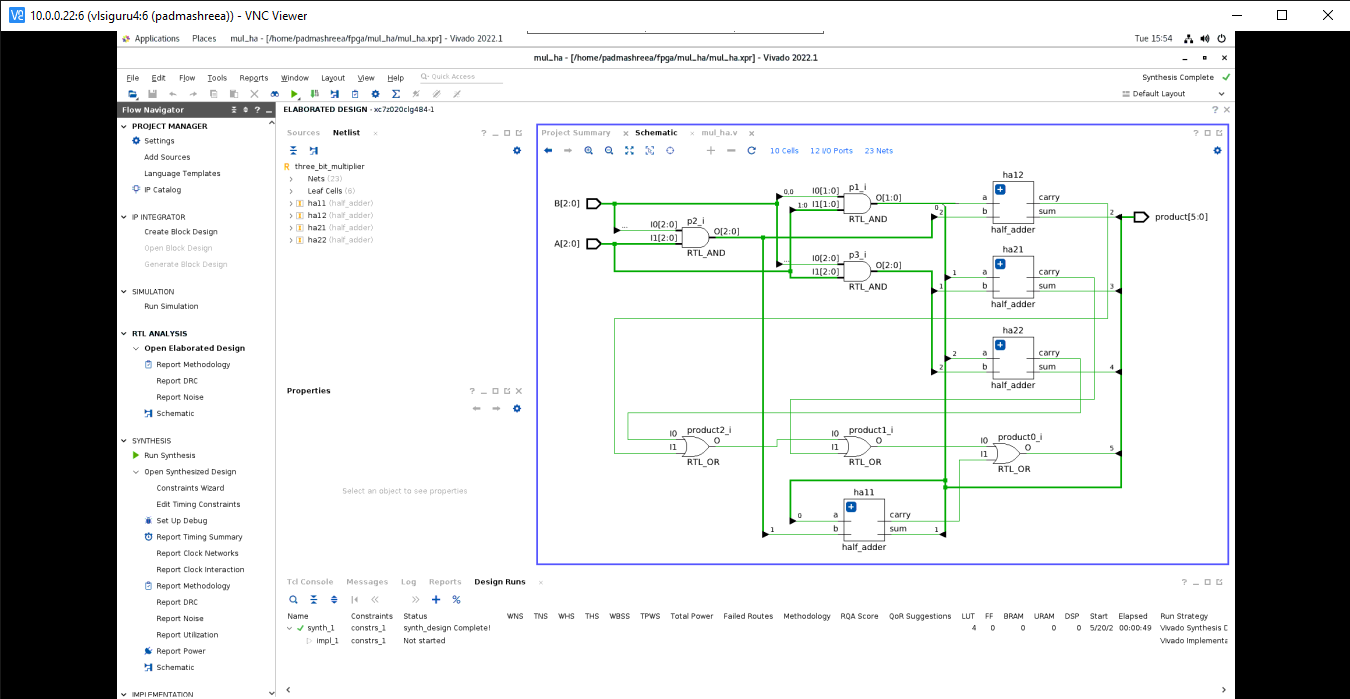
**RTL/Verilog code:**

****

**Schematic diagram:**

****

**Elaborated circuit diagram:**

****